Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-30. (Cancelled)

31. (Previously Presented) An integrated circuit comprising:

a programmable logic array (PLA) depopulated to include programmable connections only where required to implement certain known functionality and selectively minimally repopulated to accommodate future programming of other functionality.

32. (Original) The integrated circuit of claim 31, wherein:

the PLA programmed with the known functionality has certain performance characteristics, and wherein the PLA programmed with other functionality has the same performance characteristics.

33. (Original) The integrated circuit of claim 31, wherein:

the programmable connections include a storage device and a logic gate;

the PLA includes product terms and sum terms formed with gate trees.

34. (Original) The integrated circuit of claim 33, wherein:

the storage device is one of a latch or a flip-flop; and

the logic gate is an OR gate.

35. (Original) The integrated circuit of claim 33, wherein:

the storage device is one of a latch or a flip-flop; and

the logic gate is a multiplexer.

36. (Original) The integrated circuit of claim 31, wherein:

the programmable connections include a pair of storage devices and a multiplexer.

37. (Original) The integrated circuit of claim 31, wherein the PLA includes:

an AND array with a first type of programmable connection; and

an OR array with a second type of programmable connection.

38. (Original) The integrated circuit of claim 31, wherein the PLA includes:

an AND array with programmable connections that each include a pair of storage devices and a multiplexer; and

an OR array with programmable connections that each include only one storage device and a logic gate.

39. (Original) The integrated circuit of claim 31, wherein the PLA includes:

programmable connections for shared terms, spare terms, and complemented terms.

40. (Previously Presented) An integrated circuit comprising:

a programmable logic array (PLA) having a depopulated array that includes programmable connections only where required to implement certain known functionality and selectively minimally repopulated to accommodate future programming of other functionality.

41. (Original) The integrated circuit of claim 40, wherein the depopulated array is an AND array.

42. (Previously Presented) The integrated circuit of claim 40, wherein the depopulated array is an OR array.

43-47. (Cancelled)

48. (Previously Presented) A programmable logic array (PLA) comprising:

an AND array that includes a first type of programmable connection; and

an OR array that includes a second type of programmable connection;

wherein the first type of programmable connection includes a pair of storage devices and a multiplexer; and

wherein the second type of programmable connection includes only one storage device and a logic gate.

49-53. (Cancelled)

54. (Currently Amended) ~~The integrated circuit of claim 51~~ An integrated circuit comprising:

a programmable logic array (PLA) having a depopulated array that includes programmable connections only where required to implement certain known functionality, wherein the PLA includes:

programmable connections that include a storage device and a logic gate; and

product terms and sum terms formed with gate trees.

55. (Currently Amended) ~~The integrated circuit of claim 51~~ An integrated circuit comprising:

a programmable logic array (PLA) having a depopulated array that includes programmable connections only where required to implement certain known functionality, wherein the PLA includes programmable connections that include:

a pair of storage devices; and

a multiplexer.

56. (Currently Amended) ~~The integrated circuit of claim 51~~ An integrated circuit comprising:

a programmable logic array (PLA) having a depopulated array that includes programmable connections only where required to implement certain known functionality, wherein the PLA includes:

an AND array that includes programmable connections that each include a pair of storage devices and a multiplexer; and

an OR array that includes programmable connections that each include only one storage device and a logic gate.